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Air Traffic Business Division

ECMA-253 Interface Converter/ Octet Timing Regenerator

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Cautions and Notes

The following symbols are used in this guide:

CAUTION. This indicates an important operating instruction that should be followed to avoid any potential damage to hardware or property, loss of data, or personal injury

GENERAL INFORMATION

The product described in this document is an electronic system implemented in a way to guarantee a secure operation, provided that it is installed and used in conformance with the general safety standards, paying attention to the indications supplied by the supplier.

Any use different from that (or those) foreseen by the supplier are strictly forbidden.

The following provides information concerning the compliancy of the system to the safety standards, to the potential risks related to its use as well as the precautions to be adopted to avoid or limit these risks to a minimum.

EUROPEAN UNION DECLARATION OF CONFORMITY

JSP Teleconsultancy declares that the product "**ECMA 253 converter**" conforms to the CE directive 1999/05/CE of the European Parliament and the European Commission dated 9th of March 1999 for radio equipment and for telecommunications terminal equipment and the reciprocal recognition of their conformity.

This is to certify that, when installed and used according to the instructions in this manual, together with the specified cables and the maximum cable length <3m, the Units are shielded against the generation of radio interferences in accordance with the application of Council Directive 89/336/EEC as well as these standards:

EN 55022: 1999 Class B

EN 55024: 1999

IEC 61000-4-2: 2001
IEC 61000-4-3: 2001
IEC 61000-4-4: 2001

EN 61000-3-2 2001

EN 61000-3-3 2002

The equipment was tested in a typical configuration with a HP PT502 Protocol Tester.

CE

ELECTROMAGNETIC COMPATIBILITY

The equipment is compliant with all appropriate European Safety (CE etc), Electromagnetic Compatibility and Approval Requirements;

WARNING. This is termed a Class A equipment.
In a residential environment this equipment can provoke radio disturbances. In this case it can be required that the user takes adequate precautions.

ENVIRONMENTAL IMPACTS AND END OF LIFE-CYCLE DISPOSAL

Life-cycle time

No environmental impact problems exist during the normal operation of the equipment.

End of life-cycle: disposal

The product, at the end of its life-cycle must not be disposed of in the environment; its disposal must occur according to article 13 of the Law Decree 25th July 2005, n. 151 “Implementation of the directive 2002/95/CE, 2002/96/CE and 2003/108/CE, relative to the reduction in the use of dangerous substances in electrical and electronic equipment, as well as the disposal of refuse”.

The crossed refuse bin symbol shown on the equipment or on its packing and also in the following figure, indicates that the product at the end of its useful life must be collected separately from other refuse.

The differential collection of this equipment when it has reached the end of its life-cycle is organized and managed by the supplier. The user that wants to dispose of this equipment must contact the supplier and follow the method that they have adopted for the separated collection of the equipment that has reached the end of its life-cycle.

A suitable separated collection to start off the process of equipment recycling, its treatment and a compatible environmental disposal helps to avoid possible negative effects on the environment and on health, and encourages the reuse and/or recycle of the materials forming the equipment.

The abusive disposal of the product by the owner brings the application of administrative sanctions defined by the laws in force.

During the disposal process the following classification applies:

- Electronic cards: are classified according to the European code (CER) as "special refuse" code 160202.

NOTE: Some electronic cards contain capacitors of a large size; these capacitors do not contain dangerous elements like PTC or PCB, however the cards on which they are installed enter in the above cited category;

WARNING: The management of refuse must conform to the Dlvo. n.22/ 1977.

Batteries

No batteries or cells are contained within the ECMA 253 converter.

SAFETY PRECAUTIONS AND INSTALLATION GUIDELINES

To ensure reliable and safe long-term operation, please read the following safety instructions before using the ECMA 253 converter rack equipment or G.703-EIA530 converter module unit. note the following installation guidelines:

- Read the user instructions carefully and keep them in a safe place.
- Do not open the equipment, this should be performed only by specialized technical staff.
- Position the G.703-EIA530 table top module unit on a flat non-slip surface.
- Only operate this system in dry, indoor environments.
- The G.703-EIA converter modules and power supply module within the rack can get warm. Do not locate them in an enclosed space without any air ventilation.
- Do not expose the equipment to direct sun light or other heat sources.
- Do not position a heat source (e.g. another power supply) directly on top of the rack.
- Do not obstruct the rack's ventilation holes.
- Do not install or use the equipment in areas where there is risk of explosion.
- Protect the equipment from condensation, humidity, water, gases, dust and aggressive chemical liquids.
- Do not expose the equipment to electromagnetic fields (electric motors, electrodomestic appliances). Their exposure could cause a reduction in the quality of the signal.
- Avoid the use in the immediate vicinity of television, radio and video equipment.
- Do not use the equipment if you are in contact with water or have wet hands.
- The equipment can be cleaned, after disconnecting it, with a lightly damped or antistatic soft cloth.

- To clean the equipment do not use detergents, dilutions, alcohol, petrol, or other chemical substances.
- Use the equipment within an environmental temperature range of +0°C to +50°C.

Warning! For equipment connected to the mains power outlet: the mains power outlets must be installed close to the equipment and be easily accessible.

To safeguard against personal injury and avoid possible damage to equipment or property, please observe the following:

- **Only use power supplies originally supplied with the product or manufacturer-approved replacements. Do not attempt to dismantle or repair any power supply. Do not use a power supply if it appears to be defective or has a damaged case.**

- **Connect all power supplies to grounded outlets. In each case, ensure that the ground connection is maintained from the outlet socket through to the power supply's AC power input.**

- **Do not attempt to modify or repair this product**

CHANGE HISTORY

Edition	Date	Description of change
1.0	15.10.2007	

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ABBREVIATIONS

AT	Access and Terminals
ATS	Air Traffic Services
ATS-QSIG	Air Traffic Services- QSIG
COTS	Common Off The Shelf
DCE	Data Communication Equipment
DSS1	Digital Subscriber Signalling System No.1
DTE	Data Terminal Equipment
DUT	Device Under Test
ECMA	European Computer Manufacturers Association
EIA	Electronic Industries Alliance
EMC	Electro-Magnetic Compatibility
EMU	Emulation
EN	European Norm
ETSI	European Telecommunication Standards Institute
FPGA	Field Programmable Gate Array
HDLC	High-level Data Link Control
ICAO	International Civil Aviation Organisation
ISDN	Integrated Services Digital Network
ISO	International Standards Organisation
ITU-T	International Telecommunication Union – Telecom
LAP-D	Link Access Procedure on the D-channel
LD-CELP	Low Delay- Code Excited Linear Prediction
LED	Light Emitting Diode
MON	Monitor
OCT	Octet
ONP	Open Network Provision
PINX	Private Integrated Network eXchange
PISN	Private Integrated Services Network
PSS1	Private Signalling System No.1
PTN	Private Telecommunication Network
PWR	Power
Rx	Receive
Tx	Transmit
VCS	Voice Communication System

REFERENCES

For the purposes of this document, the following references apply:

1 **EN 300 290 (July 2001) – Access and Terminals (AT): 64 kbit/s digital unrestricted leased line with octet integrity (D64U) Terminal equipment interface-** Specifies the physical and electrical characteristics (except safety, overvoltage and EMC aspects) and corresponding test principles for a terminal equipment interface for connection to the network termination points of ONP 64 kbit/s digital unrestricted leased lines with octet integrity.

2 **EN 300 288 (July 2001)** – **Access and Terminals (AT): 64 kbit/s digital unrestricted leased line with octet integrity (D64U)- Network Interface Presentation** – Specifies the technical requirements and test principles for the network interface presentations of Open Network Provision (ONP) 64 kbit/s digital unrestricted leased lines with octet integrity. These presentations are codirectional.

3 **EN 300 289 (July 2001) – Access and Terminals (AT): 64 kbit/s digital unrestricted leased line with octet integrity (D64U) –Connection Characteristics-** Specifies the technical requirements and test principles for the connection characteristics of ONP 64 kbit/s digital unrestricted leased lines with octet integrity. The leased line provides access to the full digital bit rate of 64 kbit/s, with network timing for both directions of the transmission, with no restrictions on the binary content.

4 **ECMA 253 standard – "Mapping/16" (Dec 1996); "Private Integrated Services Network (PISN) – Mapping Functions for the employment of 64kbit/s Circuit Mode connections with 16 kbit/s sub-multiplexing"-** Defines the mapping functions in exchanges of Private Integrated Services Networks (PISNs) required for the utilisation of scenarios in which 64 kbit/s circuit mode connections are sub-multiplexed into 4 x 16 kbit/s channels for carrying inter-PINX signalling and user information.

5 **ITU-T Rec. G.703 – Physical/Electrical characteristics of hierarchical digital interfaces – Paragraph 1 - Interface at 64 kbit/s.**

6 **The ITU-T Recommendation G.728** contains the description of an algorithm for the coding of speech signals at 16 kbit/s using low-delay code excited linear prediction (LD-CELP).

7 **EN 300 402-2 (Nov 1995) - Integrated Services Digital Network (ISDN); Digital Subscriber Signalling System No. one (DSS1) protocol; Data link layer; Part 2: General Protocol specification –** These two ETSI standards describe in general terms the link access procedure of the Digital Subscriber Signalling System No. one (DSS1) protocol when used in the pan-European Integrated Services Digital Network (ISDN) as provided by European public telecommunications operators, or in a Private Telecommunication Network (PTN), at the T reference point or the S reference point or the coincident S and T reference point.

8 **ITU-T Rec. Q.921 "DIGITAL SUBSCRIBER SIGNALLING SYSTEM NO. 1 (DSS1) ISDN USER-NETWORK INTERFACE DATA LINK LAYER SPECIFICATION (Sep 1997) -** This Recommendation specifies the frame structure, elements of procedure, format of fields and procedures for the proper operation of the Link Access Procedure on the D-channel, LAPD.

1. INTRODUCTION

1.1 ECMA-253 converter rack general description

This document is a technical description of the ECMA-253 converter rack (Product Code: JSP101) designed and developed by JSP-Teleconsultancy.

The ECMA-253 converter rack has a height of 3U and is rack mountable system containing 6 slots. The rack contains the following modules:

- 1 x power supply module able to supply power to a fully loaded rack.
- 2 x G.703-EIA530 converter modules
- 3 x empty slots for insertion of further G.703-EIA530 converter modules or 3 channel LD-CELP audio monitoring module.

The G.703-EIA530 converter module itself is available either as a 3U (160mm by 100mm) module for insertion within the ECMA 253 converter rack or is available as a standalone table top 3U module unit with external AC/DC power adapter. The rear of the G.703-EIA530 converter module has a removable 5 screw terminal block for the G.703 co-directional Tx and Rx line pairs/ground connection and also a EIA-530/DB25 female socket for connection to a PT50X protocol tester.

The front panel of the G.703-EIA 530 converter module has a rotary switch allowing selection of Emulation, OFF, Monitor modes and an Octet Timing Regeneration mode (Option). Five luminous indicators on the module's front panel indicate the Power ON state, Rx line activity, Tx line activity, Octet Timing Sync and HDLC Sync.

1.1.1 G.703-EIA530 converter module functional modes

The G.703-EIA530 converter module has been designed to operate in 3 distinct modes: Emulation, Monitor and Octet Timing Regeneration (option).

a) Emulation Mode: Allows a HP PT50x protocol tester to be synchronized to the 64kbps digital unrestricted co-directional line (D64U) connecting a single ATS-QSIG interface card positioned within a VCS. This line can be with 8KHz octet timing integrity as defined by ETSI standards EN 300 288 and EN 300 289 or can be a line without 8KHz octet timing integrity. Emulation mode is used when a protocol tester (also configured in Emulation mode), is connected to a single ATS-QSIG implementation within the VCS in order to perform conformance testing or protocol emulation tests.

b) Monitor Mode: Allows a HP PT50x protocol tester to be synchronized to the 64kbps digital unrestricted co-directional line (D64U) connecting two ATS-QSIG interface cards positioned within VCS's on each end of a link. . This line can be with 8KHz octet timing integrity as defined by ETSI standards EN 300 288 and EN 300 289 or can be a line without 8KHz octet timing integrity. Monitor mode is used when a protocol tester (also configured in Monitor mode) is connected to one of the line's end points in order to perform layer 2 and layer 3 protocol Interoperability testing between ATS-QSIG interfaces.

c) Octet Timing Regeneration Mode (Option): Allows re-generation of an 8KHz octet timing signal from a incoming 64kbps digital unrestricted co-directional line without such a timing signal, but containing HDLC flags in its 16kbps D_Q signalling channel.

1.1.2 G.703-EIA530 converter module technology

The G.703-EIA530 converter module is a 3U module comprising of a 6 layer printed circuit board with surface mount technology and a FPGA (Field-programmable gate array) semiconductor device containing programmable logic. Through an on-board port it is possible for the supplier to re-program the FPGA with future enhanced functionality and updates.

The on-board FPGA device utilizes a combination of non-volatile FLASH cells and SRAM technology to deliver a single-chip solution supporting "instant-on" start-up and infinite re-configurability. A non-volatile FLASH cell array distributed within the FPGA device stores the device configuration. At power-up the configuration is transferred from FLASH memory to configuration SRAM in less than 1mS providing an instant-on FPGA. In addition, FPGA devices provide security by eliminating the need for an external configuration bit-stream and by providing non-volatile security features.

1.2 ECMA 312 standard (ATS-QSIG)

Eurocontrol has developed a digital signalling protocol, known as 'ATS-QSIG', to meet the ground telephone requirements of air traffic controllers in carrying out their duties of air traffic management. Eurocontrol has sponsored this protocol through the European Standardisation procedures and it has been approved and published by both ECMA-International as the ECMA 312 standard and by ETSI as the EN 301 846 standard.

ATS-QSIG was developed from an existing telecom industry standard known simply as QSIG/PSS1. ICAO recommends PSS1 for use as a digital signalling protocol and quotes ATS-QSIG as a variant that may be used in the European Region and elsewhere.

1.2.1 ECMA 253 – 16kbit/s sub-channel mapping

The ECMA 312 standard defines use of the Mapping Functions for the employment of 64kbit/s Circuit Mode Connections with 16kbit/s Sub-multiplexing by reference to the ECMA 253 standard. The ECMA-253 standard maps four 16Kbps sub-channels on a 64 Kbps bearer channel by sequentially grouping the octet aligned bits in groups of 2. The first 2 bits are the signalling D_Q channel and the next groups of two bits are the user channels U0, U1 and U2 which are each typically a voice channel with voice compression as defined by the ITU-T G.728 recommendation (LD-CELP). Refer to APPENDIX E. ECMA 253 16KBIT/S SUB-CHANNEL MAPPING.

The G.703-EIA530 converter module operates synchronously with the G.703 interface at 64 Kbps and uses clock gating to provide 16 Kbps to the EIA-530 DTE interface. The 16 Kbps D channel is specified in the ECMA 253 standard as octet bits 1 and 2 on the G.703 interface.

The G.703-EIA530 converter module provides the clock signals on its EIA-530 interface port in both Emulation and Monitor Modes, i.e. a connected protocol tester is therefore configured to operate in "to DCE" mode for both emulation and monitor modes.

1.2.2 ECMA 312 - Bipolar Code violation method (8KHz Octet timing signal)

The ECMA 312 standard assumes a physical interface according to the ITU-T G.703 Co-directional 64kbps standard. This interface is bit-serial, with a code violation used as octet delimiter, also called 8KHz octet timing signal. The purpose of the octet delimiter is to enable the exact position of the bits in the 8-bit octet to be determined. For ATS-QSIG as defined by the ECMA 312 standard, it assists in determining the position of the 2-bit D-channel carrying the call setup data, and each of the 2-bit U-channels carrying the voice payload.

Refer to Appendix C. –G.703 CODIRECTIONAL CODE CONVERSION RULES.

This principle octet synchronization solution requires 64kbps digital unrestricted leased lines compliant with ETSI EN 300 288/289 in order to guarantee octet integrity during the transport of the octets between end-systems.

Even when synchronisation to the line has been achieved, the Octet timing method continuously checks the octet violations to ensure that the position of the signalling channel bits is always known.

In the case that Octet Violations are no longer detected on a link for a pre-defined period, the system switches to the HDLC flag search synchronization method and attempts to re-synchronize to the line using this method.

1.2.3 ECMA 312 HDLC flag search method

In the case that a Telecom Operator is unable to supply a 64 kbps digital unrestricted leased circuit (D64U) that guarantees octet integrity, they may offer a bit-serial circuits (e.g. data circuits), that are however unable to guarantee octet integrity. These result in the position of code violations being anywhere within the octet and hence octet integrity is lost. In this case the ECMA 312 defines a second option in order to achieve synchronization.
A search of layer 2 HDLC flags is made within the full bit-64kbps stream channel. The Signalling channel also transports HDLC flags when idle. The identification of these flags indicates the position of the 16kbps Signalling channel within the full bit-stream. Once the position of the signalling channel is recognised, it is also possible to identify the position of the voice channels. It is then possible to determine the position of the first and last bits within an octet.

Even when synchronisation to the line has been achieved, the HDLC flag search method continuously checks the bit positions to ensure that the position of the signalling channel bits is always known.

1.2.4 Bit slip recovery

The octet violation and HDLC flag search synchronisation procedures both permit recovery from slips in the 64 kbps bit stream. Both line synchronization methods continuously monitor the link and correct instantaneously for any loss of octet synchronization. Both line synchronization methods compensates for both an odd number of bit slips as well as an even number of bit slips.

When line synchronization is achieved using the Octet Timing method, bit slips do not cause a switchover to the HDLC flag search synchronization method. Similarly when a line is synchronized using HDLC flag search, bit slips do not cause a synchronization re-attempt to occur using the Octet violations.

2. SPECIFICATION

2.1 Electrical Characteristics of the G.703 codirectional interface

Interface: ITU-T G.703 co-directional interface.

G.703 Signal In and Out: 2 wire symmetrical, electrically isolated, short-circuit protected, overvoltage protected

Maximum Range: Up to 800m over 24 gauge (0.5mm)

Data Rate: 64,000 bps (on G.703 co-directional line)

Line Signal Coding: 64kbps Codirectional line code (refer to Appendix C. –G.703 CODIRECTIONAL CODE CONVERSION RULES)

Control Signals: None

Impedance: 120Ω balanced (G.703 Emulation Mode), 1.2KΩ balanced (G.703 Monitor Mode),

Clock Frequency: 64KHz +/-100ppm

"Pulse" Amplitude: 1.0V nominal +/- 10% (refer to Appendix D. Pulse MASKS for the 64kbps codirectional interface)

"Zero" Amplitude: 0V +/-0.1 V maximum (refer to Appendix D. Pulse MASKS for the 64kbps codirectional interface)

Protocol: Synchronous 16KHz (64KHz gated clock), full duplex and bi-directional monitor

2.2 Electrical Characteristics of the EIA-530 interface

Interface type: EIA-530 interface for connection to the Protocol Tester (using either DB25 to MB34 1-to-1 adapter cable or DB25 to DB37 1-to-1 adapter cable)

Connector: DB25/Female

Data Rate: 16,000 bps (containing only extracted D_Q signalling data)

Data Type: Balanced for V.35 and V.36 (RS.449)

Impedance: 120 Ω balanced (EIA-530)

2.3 Connectors

G.703-EIA530 converter module: One removable 5-screw terminal block with terminals for Transmit and Receive Pairs of codirectional interface and ground terminal;

One DB25/Female connector used to connect to PT50x protocol tester

Power Supply module connectors: One AC mains power inlet socket for connection of mains power lead (supplied)

2.4 Front panel Indicators

G.703-EIA 530 module indicators: 5 front panel LEDs: Power, Rx Signal, Tx Signal, OCT (synchronization achieved using octet violations), HDLC (synchronization achieved using layer 2 HDLC flag search method).

Rack Power Supply Module: 1 front panel LED: PWR on/off (located within button)

2.5 Front panel Switches

G.703-EIA 530 module rotary switch: 1 front panel rotary switch (used to select Emulation, Monitor, Octet Timing Regeneration and OFF modes)

Rack Power Supply module: 1 front panel PWR on/off button with orange luminous indicator

2.6 Rear panel Switches

Rack Mains power switch: 1 rear panel PWR on/off switch located above the mains power inlet.

Mains power selector: 1 rear panel 120VAC-230VAC mains selector located below mains power inlet

2.7 Synchronization delay parameters

Delay for line synchronisation using Octet violation method: 250 µs

Delay for line synchronisation using HDLC flag search method: 1 ms (detection of 2 consecutive flags)

Loss of line synchronization using HDLC flag search method: when no flag occurs in 200ms period.

Delay to synchronize to HDLC flags on non-detection of octet violations: 1 ms (detection of 2 consecutive flags)

Delay to synchronize using Octet violations when already synchronized using HDLC flag search: 250µs (on detection of two consecutive octet violations)

2.8 Layer 2 HDLC flags

The layer 2 HDLC flag detection and decoding by the G.703-EIA530 converter module complies with ETS 300 402-2 (ISDN; Digital Subscriber Signalling Systems No. One (DSS1) protocol; Data Link Layer; Part 2: General Protocol Specification- equivalent to ITU-T Recommendation Q.921 (1993), modified (1995));

2.9 Environmental characteristics

Operating ambient temperature: 0 to 50 deg. C

Storage ambient temperature: -20 deg. C to +75 deg C

Operating Relative Humidity Tolerance: 10 to 90%, non-condensing

Storage Relative Humidity Tolerance: 10 to 90%, non-condensing

2.10 Power Supply characteristics

Rack Power Supply Module: 120V - 230 VAC +/-15%, 45-55Hz, 1A

120VAC or 240VAC mains selection rotary switch (positioned below mains inlet)

Mains power supply fuse: 1,5A rating (capsule positioned below mains inlet)

Rack Power Supply Module fuse: 1,25A rating (positioned within Power Supply Module)

External AC/DC Power adapter: 230 VAC +/-15%, 45-55Hz to 9VDC/500mA (supplied only with table top G.703-EIA 530 module unit)

Rear panel earth terminal to connect rack to earth.

2.11 Dimensions and weight

Rack Size: 22.3 W x 17.8 D x 13.5 H (cm)

Rack Weight: 2 Kg (containing Power Supply module, Two G.703-EIA 530 modules);

Table top G.703-EIA 530 module unit size: 17,5 W x 13 D x 3 H (cm)

Table top G.703-EIA 530 module unit weight: 0.3 Kg (containing single G.703-EIA 530 module)

Table top G.703-EIA 530 module circuit board: 17 W x 10 D x 0.2 H (cm)

3. INSTALLATION

This section provides instructions for the mechanical and electrical installation of the ECMA 253 Converter Rack.

3.1 Site Preparation

The ECMA 253 Converter rack (Product code JSP 101) has a height of 3U and is supplied with a mounting kit in order that it can be installed within a 19 inch Cabinet. Ensure that the ECMA 253 Converter rack has easy accessibility to a 220 VAC mains power outlet.

When a PT50x protocol tester is to be used for conformance or interoperability testing, ensure that the PT50x Protocol tester is situated within close proximity of the ECMA-253 converter rack.

Two DB25 to MB34 1-to-1 adapter cables or two DB25 to DB37 1-to-1 adapter cables are supplied in order to connect an EIA-530 port on each of the G.703-EIA 530 modules to the dual RS-449/V.36 or V.35 WAN ports on the PT50x protocol tester.

3.2 Mechanical Assembly

The ECMA 253 Converter rack is a shelf with integrated power supply that has been designed to be mounted in a 19 inch cabinet. This version is delivered completely assembled, but will need to be mounted within a 19 inch rack by an authorised technician. It is also necessary to ensure that the rack's earth terminal positioned on its rear panel is connected to ground.

The G.703-EIA 530 module unit is a single G.703-EIA 530 module that has its own casing and is externally powered through a power adapter. This unit is delivered completely assembled and has been designed as a table top version.

3.3 Electrical Installation

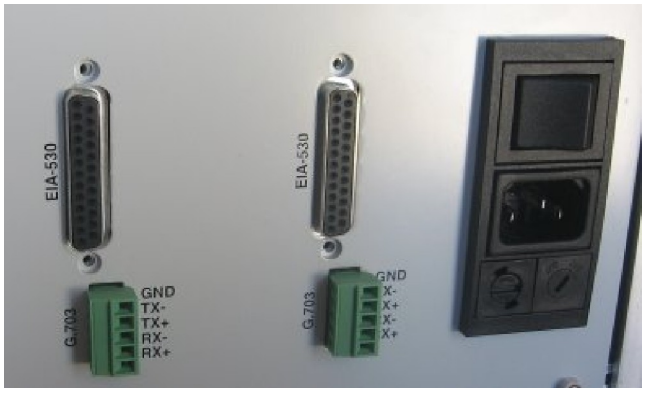

Figure 1: ECMA 253 converter rear panel view

3.3.1 Power Connection

Power is supplied to the ECMA 253 converter rack through a 230VAC/120VAC mains power inlet. A rotary switch positioned under the mains inlet selects either a 120VAC or 240VAC mains source. The mains power lead supplied is used to connect to rack to the mains power plug. Power to the shelf should be switched on via the Power ON/OFF switch situated above the mains power inlet. A replaceable fuse is situated in a capsule below the mains power inlet.

Figure 2: Mains power inlet and Power lead

3.3.2 EIA-530 Connection

Only the data, clock and grounding pins are employed on this connection. No external (DTE) clocking mode is provided. Refer to APPENDIX A. PIN CONNECTIONS FOR EIA-530 ß à V.36 (RS-449) CONVERSION ADAPTER CABLE or APPENDIX B. PIN CONNECTIONS FOR EIA-530 ß à V.35 (M/34) CONVERSION ADAPTER CABLE supplied with this unit.

Any other cable used with this unit must be 0.5 m or shorter otherwise the cable must provide balanced termination on all pairs as per ITU-T V.11 when the protocol tester is in monitor mode. If another cable is used, it must provide adequate shield ground continuity for safety purposes.

Figure 3: Rear panel EIA-530 Connector

Figure 4: V.35 (MB37) to EIA-530 adapter cable

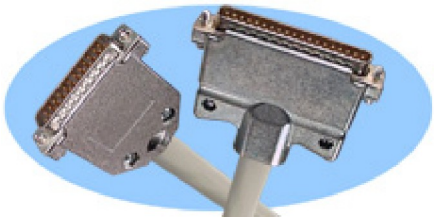

Figure 5: V.36/RS449 (DB37) to EIA-530 adapter cable

CAUTION. The EIA-530 cable connection to the PT50x RS-449/V.36 or V.35 port must be made before connecting the G.703 co-directional line. The unit's protective ground is provided by the PT50x Tester, through the specially made EIA-530 (DB25) to RS-449/V.36 (DB37) or V.35 (MB34) cable provided.

3.3.3 G.703 Co-directional line connection

The 5-screw terminal block positioned on the rear of the G.703-EIA 530 module provides 4 terminals for connecting the transmit and receive twisted-pairs of the Co-directional line. All Transmit and Receive pairs are polarity insensitive. The terminal block also contains a terminal for connection to Ground. It is recommended that connections made to the G.703 interface should be performed by a qualified technician.

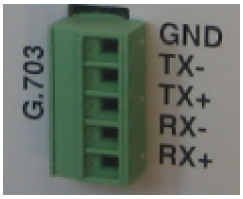

Figure 6: Rear panel G.703 codirectional line terminal block

When the G.703-EIA530 converter module is set to emulation mode, the Co-directional transmit data are connected to the G.703 TX- and TX+ terminals and the Co-directional receive data are connected to the G.703 RX- and RX+ terminals. This is illustrated in the Figure 7 below:

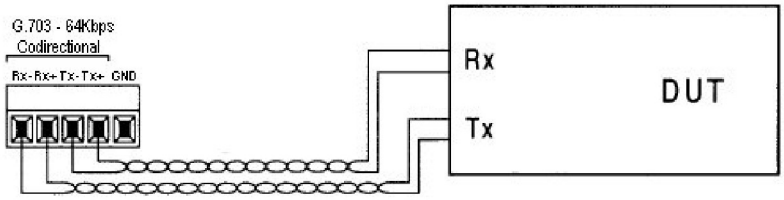

Figure 7: Connection to G.703 codirectional terminal block for Emulation mode

When the G.703-EIA 530 converter module is set to monitor mode, the G.703 TX-/TX+ and RX-/RX+ terminals are placed in high impedance mode allowing them to be connected directly to an existing line in a T-tap arrangement. In this mode the Co-directional twisted pair in one direction is connected to TX-/TX+, while the Co-directional twisted pair in the opposite direction is connected to RX-/RX+. This is illustrated in Figure 8 below:

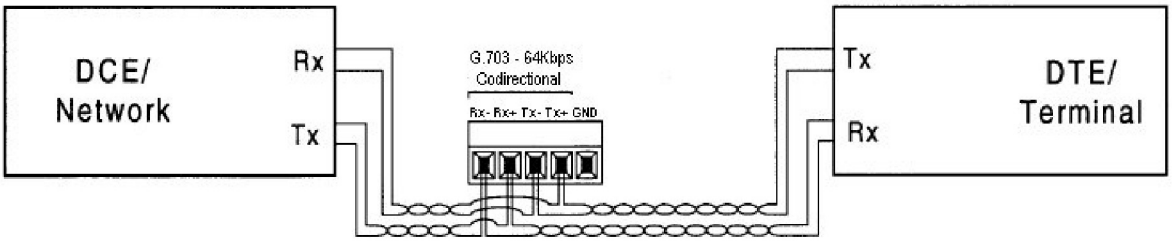

Figure 8: Connection to G.703 codirectional terminal block for Monitor mode

When the G.703-EIA 530 converter module is set to Octet Timing Regeneration mode, the co-directional receive data without octet timing integrity is connected to the G.703 RX-/RX+ terminals. The TX-/TX+ terminals output identical data to that received, but with octet timing integrity. This is illustrated in Figure 9 below:

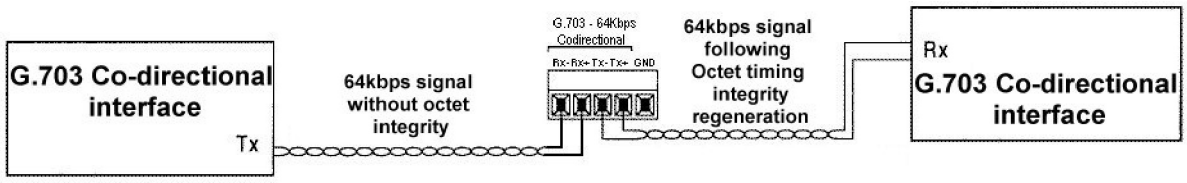

Figure 9: Connection to G.703 codirectional terminal block for Octet timing regeneration mode

Note: It is necessary for the data stream received by the G.703-EIA530 converter module to contain layer 2 HDLC flags. In the case that the receive data already contains octet timing integrity, the converter will recognise this and output on it's transmit path identical data with the same octet integrity.

4. OPERATION

Figure 10: Front Panel View

4.1 Switch Settings

Table 1: Rotary Switch settings

Rotary Switch Position	Function
MON	Selects Monitor mode
OFF	Switches the module OFF LINE mode (no mode selected).
EMU	Selects Emulation mode
OCT (indicated on G.703-EIA 530 module with Octet timing regeneration option)	Selects Octet Timing Regeneration mode

4.2 LED indicators

Table 2: Front panel LED indications

Indicator	Function
PWR	When ON indicates the module is powered-up. When the rotary switch is set to OFF, this LED is also OFF.
TX	**Emulation mode:** When ON indicates that a valid data signal is being sent on the line together with integrated 8KHz Octet timing signal. **Monitor mode:** When ON indicates that a valid data signal has been detected on the line in one direction.
RX	**Emulation mode:** When ON indicates that a valid data signal is being received from the line. **Monitor mode:** When ON indicates that a valid data signal has been detected on the line in one direction.
OCT	**Emulation mode:** When ON indicates that Timing Synchronization with the line has been achieved in the receive direction using octet violations identified within the co directional line signal. **Monitor mode:** When ON indicates that Timing Synchronization with the line has been achieved in one direction of the codirectional line through the identification of octet violations.
HDLC	**Emulation mode**: When ON indicates that Timing Synchronization with the line has been achieved in the receive direction by using the layer 2 HDLC flags search method. **Monitor mode:** When ON indicates that Timing Synchronization with the line has been achieved in one direction of the codirectional line through layer 2 HDLC flags search method.

4.3 Synchronization procedure

The G.703/EIA 530 converter module will firstly attempt to synchronise to the line by searching for octet violations (i.e. 8KHz octet timing signal) on the received signal. If these are not present it will then automatically employ the HDLC flag search method in order to achieve synchronization. Once synchronization has been achieved the converter continuously monitors the octet violations or flags to ensure synchronisation is not lost.

When synchronized using Octet violations, should these disappear for a pre-defined time from the line coding then the G.703/EIA530 module will automatically switchover to re-achieve synchronization by employing the HDLC flag search method. Following a delay to recognise 2 consecutive HDLC flags, the line will then continue to be synchronized using the HDLC flag search

Momentary physical disconnection of the co-directional line will cause the G.703/EIA 530 converter module to initially search for octet violations, but if these are not identified within a pre-defined time, it will then automatically employ the HDLC flag search method in order to re-achieve synchronization.

The octet violation and HDLC flag search synchronisation procedures both permit recovery from an odd and even number of bit slips in the 64 kbps bit stream. When line synchronization is achieved using the Octet Timing method, bit slips will trigger synchronization to be maintained using Octet Violations and does not cause a switchover to the HDLC flag search synchronization method. Similarly when a line synchronization is achieved using HDLC flag search, bit slips will trigger synchronization to be maintained using this method and does not cause a synchronization re-attempt to occur using the Octet violations.

While in monitor mode it is possible that both the OCTET and HDLC front panel LED indicators are ON simultaneously due to octet violations being present in only one direction of the co-directional line, while the opposite direction contains flags only.

4.3.1 HDLC Flag search method

HDLC Flag search method feeds 8 different pairs of bits (i.e. bits 1 & 2, bits 2 & 3, bits 3 & 4, bits 4 & 5, bits 5 & 6, bits 6 & 7, bits 7 & 8 and bits 8 & 1) from the 64kbps channel into multiple HDLC Flag detector circuits. The bit nominated bit 1 is chosen casually from the incoming serial bit stream. Eventually only one of these 8 HDLC Flag detectors will start to detect the “01111110” HDLC flags. This detector will wait for 2 consecutive flags before indicating synchronization has been achieved. The pair of bits identified as flag carrying bits indicate the position of the signalling channel within the octet. As the 3 voice channels are always offset immediately following the signalling channel, it is also possible to identify the position of the bit pairs related to each of the 3 voice channels within the octet.

Once synchronized, the HDLC flag search algorithm employed will expect at least one flag every 200ms, otherwise it will declare that synchronization has been lost.

Refer to APPENDIX F. LAYER 2 HDLC FLAG SEARCH METHOD.

4.4 Operating Procedure

The ECMA-253 converter rack requires no operator attention once installed, except for monitoring the front panel indicators on its modules.

4.4.1 Powering-up the rack

In order to switch-on power to the rack, ensure that the 220VAC mains power lead supplied with the unit is plugged into the 220Vac mains power outlet and has its socket inserted within the mains power inlet on the rear of the rack. Switch the Power ON/OFF switch situated above the mains power inlet on the rear of the rack to its ON position.

Power-up the whole rack by pressing the front panel PWR ON/OFF button, situated on the front panel of the power supply module. The orange LED indicator within the PWR button should be alight.

Set both G.703/EIA 530 modules inserted within the rack’s backplane to either EMU, MON or OCT positions. The red PWR led indication on the G.703-EIA530 module will always be alight as it indicates the module is being powered.

4.4.2 Powering-up the G.703-EIA530 module unit

In order to switch-on power to the G.703-EIA530 converter module unit, insert the power jack from the 9V AC/DC power adapter.

Set the G.703/EIA 530 converter module to either EMU, MON or OCT positions. The red PWR led indication on the G.703-EIA530 module should now be ON.

4.4.3 Mode Settings

Changes to the Rotary Switch situated on the front panel of the G.703/EIA 530 module alters its mode of operation immediately. The following notes provide further information about the different modes:

4.4.3.1 G.703-EIA530 converter module's emulation mode (EMU)

When set for Emulation Mode, the G.703-EIA 530 converter module allows an EIA RS-449 (V36) port, or a V35 port on an HP PT50x series protocol tester, to access the 16Kbps D signalling channel on an ECMA-253 mapped 64 Kbps G.703 Co-directional interface. The G.703-EIA530 converter module employs either an 8 KHz octet timing signal received from the line or a layer 2 flag location search method (in the case that 8 KHz octet timing violations are not present) to synchronize in both directions to the co-directional line.

If the front panel Octet LED is ON, this implies that the receive path is synchronized using the Octet timing method. If the front panel HDLC LED is ON, this implies that the receive path is synchronized using the HDLC flag search method.

The G.703-EIA 530 converter module therefore performs the conversion between the G.703 64Kbps Co-directional interface and the RS-449 (V36) or V35 interface on the Protocol tester.

4.4.3.2 G.703-EIA530 converter module's monitor mode (MON)

When set for Monitor Mode, the G.703-EIA 530 converter module provides a high impedance connection to the G.703 Co-directional interface. It allows an EIA RS-449 (V36) port, or a V35 port on an HP PT50x series protocol tester, to monitor the 16Kbps D signalling channel on an ECMA-253 mapped 64 Kbps G.703 Co-directional interface connected to the line. The G.703-EIA530 converter module employs either a 8 KHz octet timing signal received from the line or a layer 2 flag location search method (in the case that 8 KHz timing violations are not present) to synchronize in both directions to the co-directional line. In monitor mode, the EIA530 transmit data signal reverses direction and is driven by the converter module.

If only the front panel Octet LED is ON, this implies that both directions are synchronized using the Octet timing method. If only the front panel HDLC LED is ON, this implies that both directions are synchronized using the HDLC flag search method. It is also possible for one direction to be synchronised using 8KHz Octet timing and the opposite direction to be synchronised using HDLC flag search. In this case both Octet and HDLC LEDs on the front panel are ON.

The ECMA-253 interface converter therefore performs the conversion between the G.703 64Kbps Co-directional interface and the RS-449 (V36) or V35 interface on the Protocol tester.

CAUTION. In order to avoid V.11 signal contention, the PT50x Protocol Tester should be put into monitor mode before switching the G.703-EIA530 module between its Emulation and Monitor modes. No damage will occur to either unit if this procedure is not followed.

4.4.3.3 G.703-EIA530 converter module's Octet regeneration mode (OCT)

When set for Octet Timing Regeneration mode (Option), the G.703-EIA 530 module is able to regenerate an 8KHz octet timing signal on its Transmit pair following reception of a valid signal without octet timing, but with layer 2 HDLC flags on its Receive Pair. The G.703-EIA 530 module employs its built-in HDLC flag search algorithm to quickly identify the position of the two D-channel bits within the octet. Once identified it is able to re-generate octet timing violations required for the 8KHz octet timing signal. This mode of operation requires that one G.703-EIA 530 module is employed for each direction.

4.5 G.703-EIA530 circuit board plugs

The following table provides information about the functional use of the six plug connectors positioned on the circuit board of the G.703-EIA530 converter module.

Table 3: G.703-EIA530 Circuit board plugs

Plug	Function
P1	Connection to FPGA re-programming tool
P2	Connection to Power Supply Module or External Power Adapter
P3	Connection to 3 LD_CELP voice channel monitor module
P4	Connection to Test Port
P5	Connection to front panel rotary switch
P6	Connection to front panel luminous LED indicators

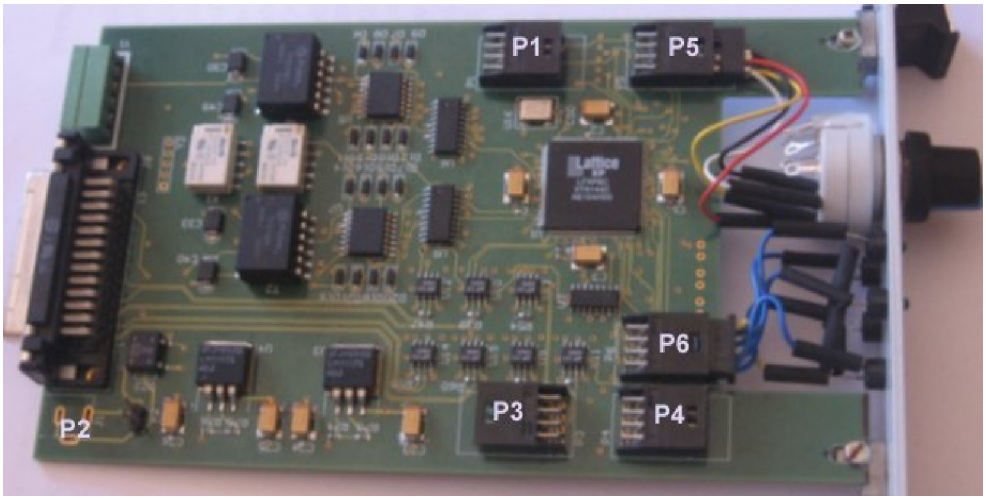

Figure 11: G.703-EIA530 converter module plug positions

APPENDIX A. Pin connections for EIA-530 ß à V.36 (RS-449) Conversion adapter cable

Part No. JSP-101-C1

EIA-530 is a balanced serial interface standard that generally uses a 25 pin connector. The EIA-530 isn't an actual interface, but a generic connector specification.

EIA-530 uses a differential signalling on a DB25 - EIA-530 Transmit (and the other signals) use a twisted pair of wires (TD+ & TD-). This interface is used for HIGH SPEED synchronous protocols. Using a differential signalling allows higher speeds over long cabling.

The RS449 interface is a generic connector specification. It's not an actual interface. The connector pinning was originally designed to support RS422 for balanced signals, and RS423 for the unbalanced signals.

RS449 is a high speed digital interface. RS449 V.11 receivers look for the difference between two wires. The differential signals for RS449 are labelled as either "A and B" or "+ and -". In the case of RS449 wire A or + does not connect to B or -. Wire A always connects to A and B connects to B or + to + and - to -.

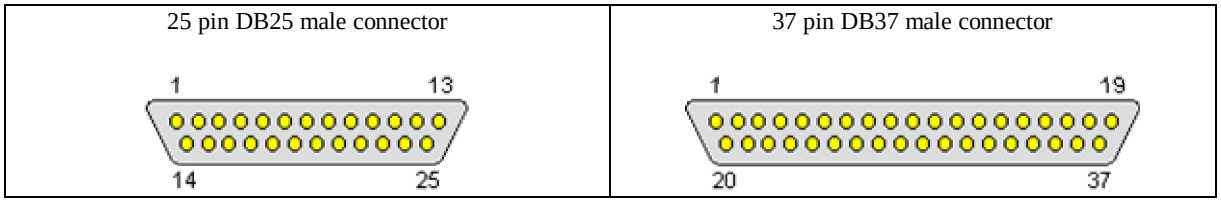

Figure 12: 25 pin DB25 male connector/37 pin DB37 male connector

Table 4: EIA 530 to V.36 cable pin outs

Signal	Pin (EIA-530/DB25)	Direction	Pin (V.36 RS-449/DB 37)	Signal
Shield	1	-	1	Shield
Transmit Data –TxD(A)	2	ß à	4	Send Data (A)
Receive Data - RxD(A)	3	à	6	Receive Data (A)
Signal Ground	7	-	19	Signal Ground
Return Receive Signal Element timing-RxC(B)	9	à	26	Receive Timing (B)
Return Transmit Signal Element Timing- TxC(B)	12	à	23	Send Timing (B)

Signal	Pin (EIA-530/DB25)	Direction	Pin (V.36 RS-449/DB 37)	Signal
Return Transmit Data- TxD(B)	14	ß à	22	Send Data (B)
Transmit Signal Element Timing- TxC(A)	15	à	5	Send Timing (A)
Return Receive Data- RxD(B)	16	à	24	Receive Data (B)
Receive Signal Element timing- RxC(A)	17	à	8	Receive Timing (A)
Signal Ground	19	-	7	Signal Ground

APPENDIX B. Pin connections for EIA-530 ß à V.35 (M/34) Conversion adapter cable

Part No. JSP-101-C2

EIA-530 is a balanced serial interface standard that generally uses a 25 pin connector. The EIA-530 isn't an actual interface, but a generic connector specification.

EIA-530 uses a differential signalling on a DB25 - EIA-530 Transmit (and the other signals) use a twisted pair of wires (TD+ & TD-) instead of TD and a ground reference as in RS232 or V.24. This interface is used for HIGH SPEED synchronous protocols. Using a differential signalling allows higher speeds over long cabling.

V.35 is a high-speed serial interface designed to support both higher data rates and connectivity between DTEs or DCEs over digital lines.
V.35 is an interface commonly used on higher speed circuits of 56kbps and above. Recognizable by its blocky, 34-pin connector; V.35 combines the bandwidth of several telephone circuits to provide the high-speed interface between a DTE or DCE and a CSU/DSU (Channel Service Unit/Data Service Unit). To achieve such high speeds and great distances, V.35 combines both balanced and unbalanced voltage signals on the same interface. Transmission is usually a synchronous protocol (note clocking pins i.e. receive and transmit clock). Although V.35 is commonly used to support speeds ranging anywhere from 48 to 64 Kbps.

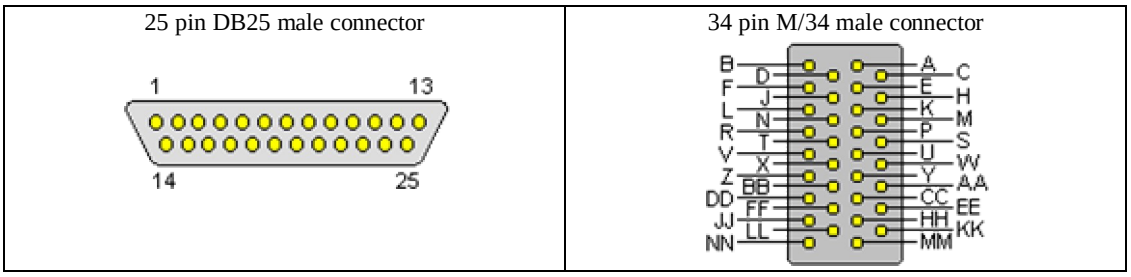

Figure 13: 25 pin DB25 male connector/34 pin M/34 male connector

Table 5: EIA 530 to V.35 cable pin outs

Signal	Pin (EIA-530/DB25)	Direction	Pin (V.35/DB 37)	Signal
Shield	1	-	A	Shield
Transmit Data –TxD(A)	2	ß à	P	Send Data (A)
Receive Data - RxD(A)	3	à	R	Receive Data (A)
Signal Ground	7	-	B	Signal Ground
Return Receive Signal Element timing-RxC(B)	9	à	X	Receive Timing (B)

Signal	Pin (EIA-530/DB25)	Direction	Pin (V.35/DB 37)	Signal
Return Transmit Signal Element Timing- TxC(B)	12	à	AA	Send Timing (B)
Return Transmit Data- TxD(B)	14	ß à	S	Send Data (B)
Transmit Signal Element Timing- TxC(A)	15	à	Y	Send Timing (A)
Return Receive Data- RxD(B)	16	à	T	Receive Data (B)
Receive Signal Element timing- RxC(A)	17	à	V	Receive Timing (A)
Signal Ground	19	-	B	Signal Ground

APPENDIX C. –G.703 CODIRECTIONAL CODE CONVERSION RULES

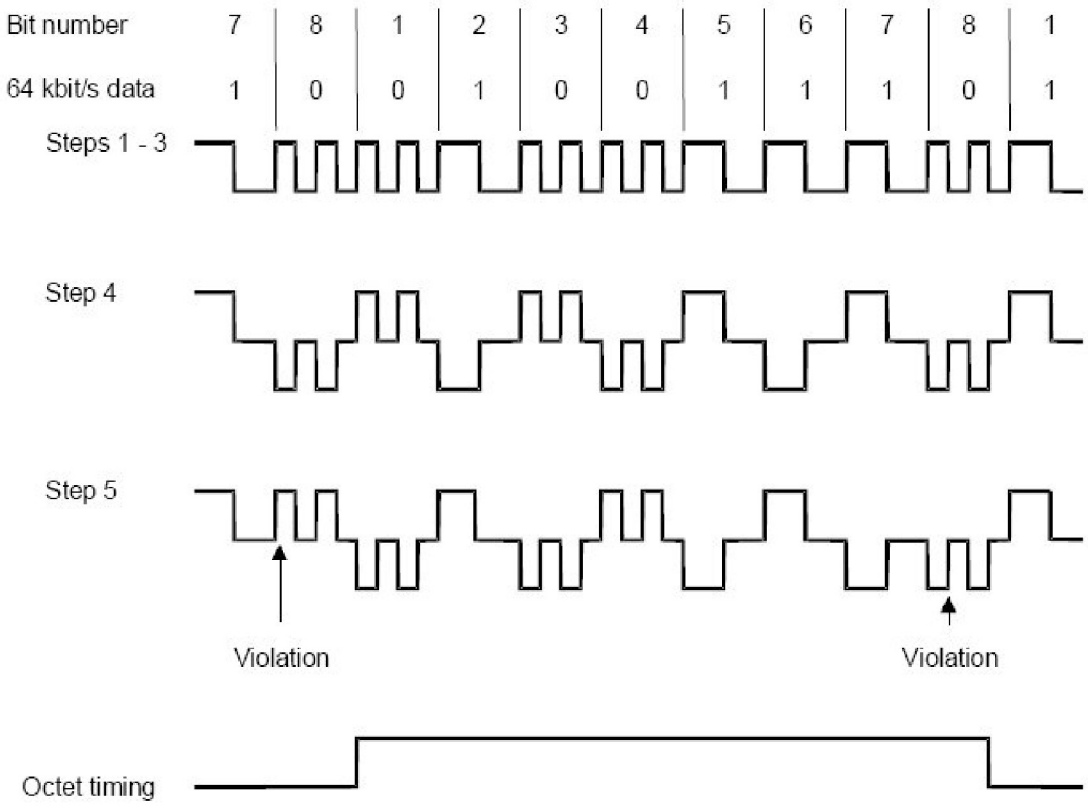

Figure 14: G.703 codirectional code conversion rules illustration

Step 1: A 64Kbps period is divided into four unit intervals.
Step 2: A binary “one” is coded as a block of four bits “1100”.
Step 3: A binary “zero” is coded as a block of four bits “1010”.
Step 4: The binary signal is converted into a three-level signal.
Step 5: A “Violation” block marks the last bit in an octet.

APPENDIX D. PULSE MASKS FOR THE 64KBPS CODIRECTIONAL INTERFACE

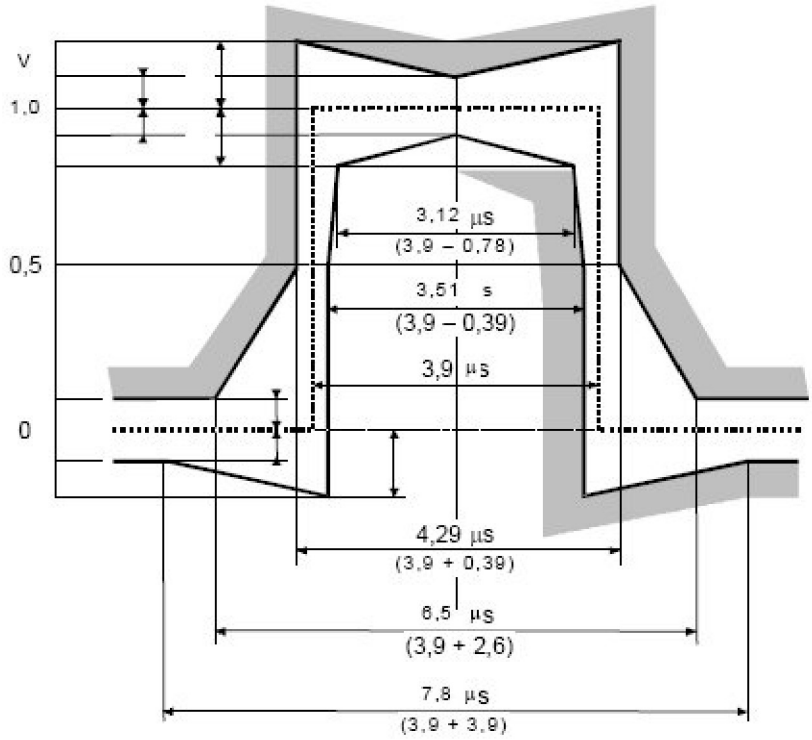

Figure 15: Mask for a single unit interval pulse

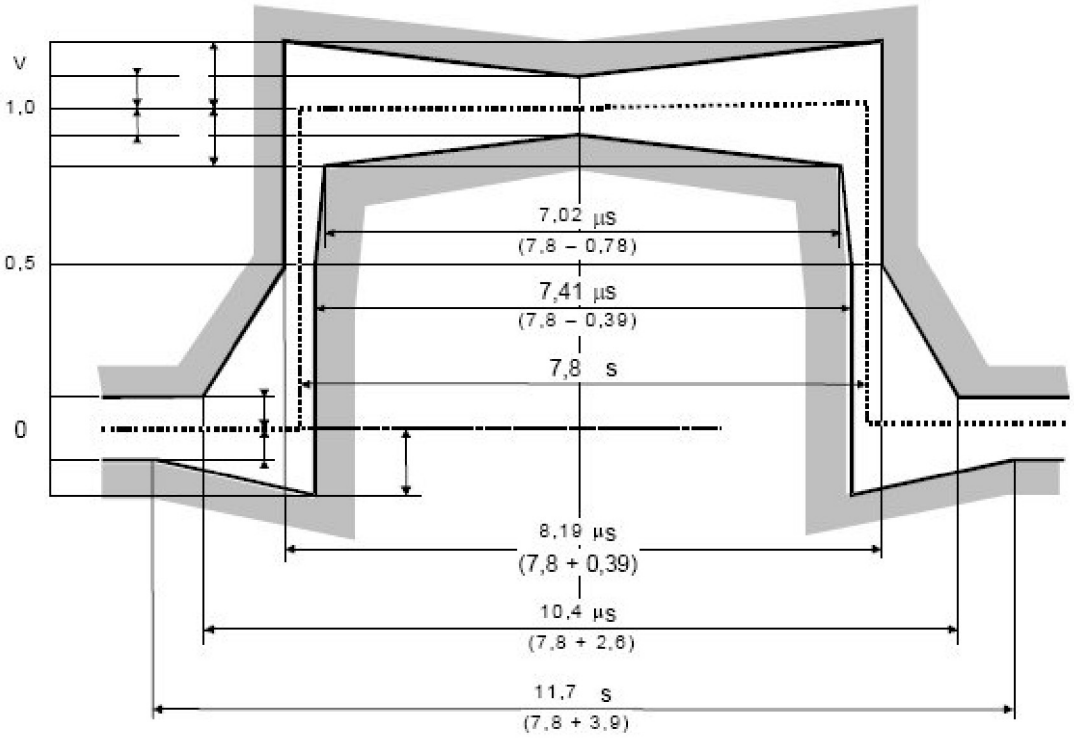

Figure 16: Mask for a double unit interval pulse

APPENDIX E. ECMA 253 16Kbit/s SUB-CHANNEL MAPPING

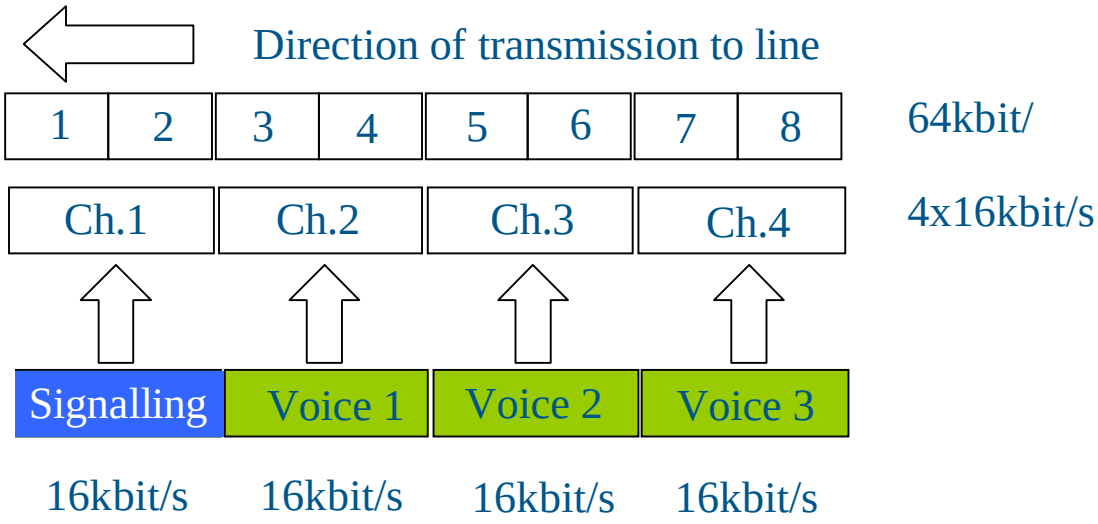

Figure 17: ECMA 253 16kbit/s sub-channel mapping

APPENDIX F. LAYER 2 HDLC FLAG SEARCH METHOD

Start search on any bit from bit stream (nominated bit 1) and direct consecutive pairs of bits to 8 flag Search detectors. Only one of the 8 Flag detectors will start to detect "01111110" HDLC flags. The figure shows that flags are detected in bits 4&5, implying bits 4&5 represent the first two bits of the octet.

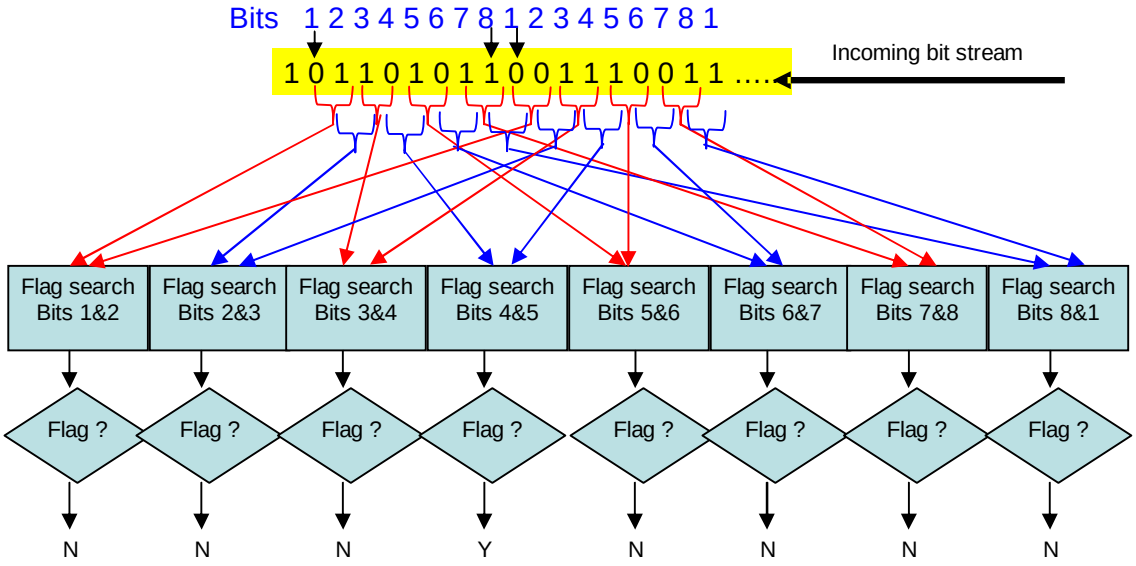

Figure 18: Layer 2 HDLC Flag Search method